

**REMARKS**

Claims 1-9 and 11-18 are pending in the application. Claims 1, 5 and 8 have been amended and claim 16 has been added by the foregoing amendment. No new matter has been introduced as a result of this amendment as support for the claim amendments may be found in the Specification (page 8, line 45 to page 9, line 5 for example).

Applicants appreciate the Examiner's suggestion that the claims be amended prior to requesting an interview to discuss the case. The claims have been amended.

While preparing the previous response (on October 31, 2007), the undersigned was unable to communicate with the Examiner as the Examiner's voicemail message indicated that the Examiner was out of the office for several weeks (until December 2007). As a result of the Examiner's unavailability, the undersigned contacted the Examiner's Supervisor by telephone (Mr. David Wiley who apparently is no longer the Examiner's Supervisor) to request an interview to discuss the application.

Due to the approaching six month date, a RCE was filed on October 31, 2007 with the understanding (based on Mr. Wiley's statement) that an opportunity to discuss the case would be provided prior to an issuance of the Office Action. However, no communication was received prior to issuance of the pending Final Office Action, to set up an interview.

Accordingly, the undersigned again requests that an interview be granted, prior to an examination by the Examiner, to discuss the case.

Claims 1-9 and 11-14 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent No. 6,338,078 ("Chang").

Exemplary embodiments are directed to a method for controlling the order of datagrams being processed by at least one processing engine having at least one input port and at least one output port. As recited in amended claim 1 for example, the method comprises the steps of:

- (a) each processor in the at least one processing engine, once it becomes available, taking a ticket from a ticket dispenser, the ticket having a value associated therewith;
- (b) waiting on an input buffer of the input port until the processor is given permission to continue according to the value of the ticket taken in step (a);
- (c) reading a next datagram or group of datagrams once the processor is given permission to continue;
- (d) signaling the input buffer for next ticket value;
- (e) processing the read datagram by the processor;
- (f) waiting on an output buffer of the output port until the processor is given permission to continue according to the value of the ticket taken in step (a);
- (g) writing the processed datagram once the processor is given permission to continue;
- (h) signaling the output buffer for next ticket value; and
- (g) repeating steps (a)-(h) for each ticket value.

Claim 1 has been amended to more clearly recite the processors being controlled by tickets. The processors wait until their ticket is called to process datagrams. As highlighted previously, exemplary embodiments facilitate any processor, upon becoming available, taking a next datagram for processing. Chang describes having a dedicated queue (62-68) corresponding to each processor (54-60) such that a processor (such as processor 60 for example) can only process data in queue 68 and not data in other queues (such as 62, 64 or 66) even if processor has completed processing of the data in its queue (i.e. 68).

The distinctions in exemplary embodiments over the teachings of Chang have been

highlighted previously. The claims have been amended herewith to more clearly distinguish Applicant's method and system over Chang.

Chang is concerned with preserving packet order in a computer network system. In contrast, according to exemplary embodiments, any processing element can process any packet in the queue and can distribute that packet to any client device in accordance with the packet header.

In exemplary embodiments, incoming packets are allocated tickets by a ticket dispenser where the ticket represents the arrival time of the packet. The packets wait in queue while processing elements complete processing preceding packets. Upon completing the processing of a preceding packet, the processing element processes the packet associated with the next ticket. There is no need for the processing element to process a whole batch or queue of tickets as in Chang before seeking the next ticket. All the processing elements operate in this manner. Therefore, although the packets are fetched from the queue in their arrival order, they may be processed faster (or slower) than others, depending the nature of the process. As a result, packets may actually exit the processor in an order that is different from the arriving order/time. Exemplary embodiments, however, use the ticket to control the order of the packets at the at least one input port and the at least one output port.

Chang fails to disclose or suggest the processors, once they become available, taking the next ticket to process the associated datagram (packet).

Chang processes all the packets in a queue and then the CPU responsible for processing the packets in its queue has no more packets to process until more packets arrive and are

sent/placed in a queue for this CPU by a hashing function. Chang does not permit a CPU to begin processing packets in other queues (i.e. other than the queue assigned/associated to this CPU).

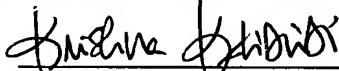
At least for these reasons, it is believed that claims 1, 5 and 8 are allowable over the teachings of Chang. The remaining claims (i.e. claims 2-4, 6, 7, 9 and 11-14), all of which depend on one of allowable independent claims 1, 5 and 8 are also allowable.

In addition, new claims 16-18 (also dependent on allowable claim 1) and amended claim 15 highlight additional advantageous aspects of exemplary embodiments.

All of the rejections having been overcome, it is believed that this application is in condition for allowance and a notice to that effect is earnestly solicited.

Respectfully submitted,

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